REMARKS

Claims 1-23 were presented for examination. Claims 1-5, 11, 13-14, 19-21 and 23 were rejected as anticipated by United States Patent No. 5,694,583 to Williams et al. ("Williams"). Claims 6-9 were rejected as obvious over Williams in view of United States Patent No. 5,383,161 to Sanemitsu ("Sanemitsu"). Claims 10, 15, and 22 were rejected as obvious over Williams in view of United States Patent No. 5,799,324 to McNutt et al. ("McNutt"). Claims 16-17 were rejected as obvious over Williams in view of United States Patent No. 5,875,465 to Kilpatrick et al. ("Kilpatrick"). Claim 12 was objected to as depending on a rejected base claim but was deemed allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for his consideration of the Information Disclosure Statements submitted on February 26, 2001, February 4, 2002, and April 22, 2002 (Papers 4, 5, and 6, respectively) and for his careful consideration of the specification. Applicant hereby amends claims 1-2, 4-9, 11-18, and 20-23 to more clearly recite the present invention and to address the minor errors in language noted by the examiner. Support for the claim amendments may be found throughout the specification and, more particularly, at page 6, lines 5-16 of the specification. Applicant respectfully submits that the claims, as amended, distinguish patentably over the cited prior art.

Rejection under 35 USC 102(b) of claims 1-5, 11, 13-14, 19-21, and 23

Claims 1-5, 11, 13-14, 19-21, and 23 were rejected as anticipated by Williams. Of these rejected claims, claims 1, 11, 13, and 20 are independent. Claim 19 depends from independent claim 18, which was not rejected as anticipated by Williams. However, applicant will address his arguments to claim 18, as well.

Independent claims 1, 11, 13, 18, and 20 each recite a computer system having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory. The non-persistent region of volatile memory may be directly written to by the operating system and is initialized when the computer is booted. The persistent region of volatile memory is not directly written to by the

operating system and is not initialized when the computer is booted. (See Specification, pg. 5, lns. 16-21 and pg. 6, lns. 7-8 and 13-15). That is, the present invention relates to providing, in a fault-tolerant computer, a region of random access memory capable of retaining its contents upon a system crash and the ensuing boot cycle. (See Specification, pg. 3, lns. 7-9).

Williams, in contrast, does not disclose such a system. Williams discloses a boot process that may be configured to bypass initialization of at least a portion of the computer's memory. (See Williams, Fig. 11). Williams does not disclose, however, a portion of volatile memory that is not directly written to by the operating system. In fact, Williams explicitly discloses that its preservation of BIOS boot emulation parameters relies on the operating system's ability to move the parameters into a specific portion of main memory before the boot sequence commences. (See Williams, Fig. 11, step 100).

Nor does Williams suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized when the computer is booted because Williams is not concerned with preserving system state upon a system crash. Instead, Williams relies on proper functioning of the computer system to preserve boot emulation parameters across warm boots. If the computer system disclosed by Williams crashes before, or during, the boot sequence described in Fig. 11 of Williams, the emulation boot parameters will be lost.

Accordingly, Applicant respectfully submits that Williams does not teach or suggest the invention recited by independent claims 1, 11, 13, 18, and 20, that claims 1-5, 11, 13-14, 19-21, and 23 define patentably over Williams, and that those claims are now in condition for allowance.

Rejection under 35 USC 103 of claims 6-9

Claims 6-9 were rejected as obvious over Williams in view of Sanemitsu. Claims 6-9 depend from independent claim 1. The arguments presented above with

respect to the teaching of Williams apply with equal force here and are reiterated as if set forth in full.

Sanemitsu does not cure the deficiencies in the teaching of Williams. Sanemitsu is directed to an integrated circuit card that prevents easy rewriting of information stored in the card. (See Sanemitsu, col. 2, lns. 14-17). Sanemitsu does not teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized.

Both Williams and Sanemitsu fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized. Accordingly, Applicant respectfully submits that the combination of Williams and Sanemitsu does not teach or suggest the invention recited by independent claim 1, that claims 6-9 define patentably over the combination of Williams and Sanemitsu, and that those claims are now in condition for allowance.

Rejection under 35 USC 103 of claims 10, 15, and 22

Claims 10, 15, and 22 were rejected as obvious over Williams in view of McNutt. Claim 10 depends from independent claim 1, claim 15 depends from independent claim 13, and claim 22 depends from independent claim 20. The arguments presented above with respect to the teaching of Williams apply with equal force here and are reiterated as if set forth in full.

McNutt does not cure the deficiencies in the teaching of Williams. McNutt teaches a system and method for management of persistent data in a log-structured disk array in which persistent data is stored to a disk drive. (See McNutt, Abstract). McNutt does not teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating

system and is not initialized. Rather, McNutt merely teaches efficient ways to store persistent data to well-known persistent storage.

Both Williams and McNutt fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized. Accordingly, Applicant respectfully submits that the combination of Williams and McNutt does not teach or suggest the invention recited by independent claims 1, 13, and 20, that claims 10, 15, and 22 define patentably over the combination of Williams and McNutt, and that those claims are now in condition for allowance.

Rejection under 35 USC 103 of claims 16-17

Claims 16-17 were rejected as obvious over Williams in view of Kilpatrick. Claims 16-17 depend from independent claim 15. The arguments presented above with respect to the teaching of Williams apply with equal force here and are reiterated as if set forth in full.

Kilpatrick does not cure the deficiencies in the teaching of Williams. Kilpatrick teaches a cache control circuit that allows a portion of the cache to be "locked," that is, data values in the "locked" portion of the cache are not replaced when new data is stored in the cache. (See Kilpatrick, Abstract). Kilpatrick does not teach that his disclosed cache memory is not reset during a boot cycle. Nor does Kilpatrick otherwise teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized on a boot cycle.

Both Williams and Kilpatrick fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized during a boot cycle. Accordingly, Applicant respectfully submits that the combination of Williams and Kilpatrick does not teach or suggest the invention recited by independent claim 15, that

claims 16-17 define patentably over the combination of Williams and Kilpatrick, and that those claims are now in condition for allowance.

Prior art not relied upon

Applicant agrees with the Examiner that European patent publication EP 0 461 924 A2 to Kelly et al. neither teaches nor discloses the invention recited by the claims.

CONCLUSION

In view of the points above, Applicant submits that each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to reconsider the patentability of all presented claims and pass this application to allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SRT-002, from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

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